UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,886	01/16/2002	Valery V. Felmetsger	SPUTT-57354	7950

7590 01/24/2006

ELLSWORTH R. ROSTON, ESQ.
FULWIDER PATTON LEE & UTECHT, LLP
Howard Hughes Center
6060 Center Drive, Tenth Floor
Los Angeles, CA 90045

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/051,886	FELMETSGER, VALERY V.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 22-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *59-64* is/are allowed.

6)☒ Claim(s) *1,3,4,22-58 and 65-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 11/17/05 has been fully considered and made of record in the instant application. Claims 5-21 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 11/17/05 have been fully considered but they are not persuasive.

In regards the different mechanism where the present invention provides a physical RF plasma etch at high inert gas pressure with low energy ions while Matsuda et al. and Lee et al. both provide a chemical RF plasma etch. The claims are not so limited in scope since the claims do not recite a particular RF plasma. Matsuda discloses removing a thin layer (i.e. silicon oxide film) from the surface of a wafer 11 (i.e. substrate) to eliminate any impurities from the surface of the wafer and thereafter creating microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface. Microscopic roughness on the surface of the wafer is created by providing dry etching on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer (see English abstract and all figures).

In regards to Matsuda and Lee failing to employ inert gas to etch the substrate (i.e. in a physical etch mechanism). Lee is relied upon to disclose a dry etching chamber environment having ions of an inert gas of argon are used to etch a substrate (see paragraph 9-11).

In regards to the present invention having no oxidation process. The claims are not so limited in scope since the claims do recite that an oxidation process can not be used.

In regards to the present invention having a roughness of an atomic size (i.e. of 10 angstrom) to accommodate a deposited layer of a few hundred angstroms. The claims are not so limited in scope since the claims do recite the atomic size of the roughness.

Therefore, this action is made **final**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (JP 2-301133) in view of Lee et al. (US 2003/0068898).

With respect to Claims 1 and 3, Matsuda discloses removing a thin layer (i.e. silicon oxide film) from the surface of a wafer 11 (i.e. substrate) to eliminate any impurities from the surface of the wafer and thereafter creating microscopic roughness on the surface of the wafer to receive a deposition of the material (i.e. chromium) on the surface. Microscopic roughness on the surface of the wafer is created by providing dry etching on the surface of the wafer with an insufficient energy to etch the surface of the

wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer (see English abstract and all figures). Matsuda fails to explicitly disclose providing ions of an inert gas of argon to create the microscopic roughness. However, Lee discloses that in a dry etching chamber environment ions of an inert gas of argon are used (see paragraph 9-11). Thus, Matsuda and Lee have substantially the same environment of a dry etching in a polysilicon environment. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate an environment having ions of an inert gas of argon, since the argon gas would selectively and uniformly etch a polysilicon layer which enhance the semiconductor process as taught by Lee.

With respect to Claim 4, Lee discloses a wafer 16 disposed on a wafer land 14 and wherein the chromium layer of Matsuda would be deposited on the wafer land 14 of Lee after the microscopic roughness has been produced on the surface of the wafer.

5. Claims 22-58, and 65-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (JP 2-301133) and Lee et al. (US 2003/0068898) as applied to claims 1 and 4 above, and further in view of Stress Control in Multi-Layer Backside Metallization of Thinned Wafers (TW article), the Admitted Prior Art and Tailoring Sputtered Cr films on Large Wafer article (LW article).

With respect to Claims 22, 29, 32, 34, 35, 39, 42-44, 46-55, and 66-69, Matsuda-Lee discloses the claimed invention except thereafter depositing a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer with a low stress value and thereafter depositing a layer of nickel vanadium with an intrinsic stress on the

surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer. TW article discloses depositing (i.e. atomically bonding) a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer with a RF bias power and thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer (see pages 4-15). The atomic bonding is inherently produced between the chromium in the chromium layer and the microscopically rough surface of the wafer of Ueno. Thus, Matsuda-Lee and the TW article have substantially the same environment of a substrate in argon filled chamber. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the chromium and nickel vanadium on the substrate of Matsuda-Lee, since the chromium and nickel vanadium would facilitate a stress control bonding between the metals and the substrate as taught by the TW article.

With respect to Claims 24-27, 30, 31, 33, 36-38, 40, 41, 45, 65, the TW article discloses a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas argon flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm) in an environment of (5-15sccm) (see pages 4 –15 and Tables 1 and 2). Thus, the chromium is deposited on the wafer at a low rate of flow of an inert gas and wherein the RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer. It is well known in the

semiconductor industry to have a RF power or no RF power when depositing a metal layer (i.e. Chromium) as evident by LW (see page 5).

With respect to Claims 23, 28, 56-58, the TW article discloses a layer of metal selected from the group consisting of gold, silver and copper is deposited on the surface of the layer of nickel vanadium and wherein the nickel vanadium layer has a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper (see pages 9-15). It is well known to solder an electronic component to the layer of metal selected from the group consisting of gold, silver, and copper as evident by the Admitted Prior Art (see page 2).

6. Claims 70-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (JP 2-301133) and Lee et al. (US 2003/0068898) as applied to claim 1 above, and further in view of Li et al. (US 2003/0017628).

With respect to Claims 70-72, Matsuda-Lee both fail to disclose wherein the inert gas pressure is about 4×10^{-3} Torr, the inert gas flow is between 40 to 50 sccm, and the energy provided to the ions of the inert gas is between 50W to 100W. However, Li discloses wherein the inert gas pressure is about 4×10^{-3} Torr, the inert gas flow is between 40 to 50 sccm, and the energy provided to the ions of the inert gas is between 50W to 100W (see paragraphs 33-36). Thus, Matsuda-Lee and Li have substantially the same environment of cleaning the surface of a wafer. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating the inert gas having the specified pressure, flow, and energy with the process of Matsuda-Lee, since the

inert gas would facilitate the cleaning of the substrate before any deposition process as taught by Li.

Allowable Subject Matter

7. Claims 59-64 are allowed.

8. Providing a flow of an inert gas in the order of forty (40) to fifty (50) standard cubic centimeters per minute through a chamber containing the wafer to etch a microscopic layer of material with impurities from the surface of the wafer and provide an atomic roughness to-the wafer surface, thereafter providing a flow of an inert gas through the chamber at a flow rate of approximately forty (40) to fifty (50) standard cubic centimeters per minute and a power in the order of six hundred watts (600 W) to twelve hundred watts (1200 W) to clean the surface of the wafer and increase the roughness of the wafer surface, disposing the wafer on a wafer land, and then providing a flow of an inert gas at a rate through the chamber at a low power in the order of fifty watts (50 W) to one hundred watts (100 W) to provide the surface of the wafer with the microscopic roughness in claim 59.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/August 22, 2005